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Ferroelectric Transistors with Nanowire Channel: Toward Nonvolatile Memory Applications

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ABSTRACT We report the fabrication and characterization of ZnO nanowire memory devices using a ferroelectric $Pb(Zr_{0.3}Ti_{0.7})O_3$ (PZT) film as the gate dielectric and the charge storage medium. With a comparison to nanowire transistors based on SiO_2 gate oxide, the devices were evaluated in terms of their electric transport, retention, and endurance performance. Memory effects are observed as characterized by an eminent counterclockwise loop in $I-V_g$ curves, which is attributed to the switchable remnant polarization of PZT. The single-nanowire device exhibits a high (up to 10^3) on/off ratio at zero gate voltage. Our results give a proof-of-principle demonstration of the memory application based on a combination of nanowires (as channels) and ferroelectric films (as gate oxide).

KEYWORDS: ZnO · nanowires · field effect transistor · nonvolatile memory · PZT · ferroelectric · depletion

The application of semiconducting nanowires (NWs) as nonvolatile memory component (*e.g.*, field effect transistor channel) is attractive due to the intrinsic priorities of nanowires over conventional film channels. For example, with a high crystalline quality, NWs can function as a superior carrier transportation channel with an enhanced mobility. Moreover, the small dimension of NWs is desirable not only for increasing the area density of device cells but also for reducing the operating voltage effectively so that the write/erase power consumption can be lowered to about several nJ.[1,2] There have been a few reports on NW-based memory using self-assembled molecules,[1,2] high-*k* dielectrics,[3,4] and ferroelectric films[5] as the charge storage media. This brings a new and exciting application to NWs in next-generation nanoelectronics, in addition to other demonstrated applications such as nanoelectromechanical systems[6,7] and biosensors.[8−10]

Ferroelectric FET (FeFET) memory has been extensively studied as an important type of nonvolatile random access memory device, due to the switchable remnant polarization of the ferroelectric insulator.[11,12] By replacing the typical gate dielectric SiO_2 with a high-*k* ferroelectric [lead zirconate titanate (PZT) has a dielectric constant about 100 times that of SiO_2], the transconductance could be increased significantly and the subthreshold swing reduced. A combination of high-mobility semiconducting nanowires as the channel with ferroelectric film as the gate dielectric is expected to have enhanced memory performance (*e.g.*, a higher on/off ratio) compared with the conventional film FeFET.[13]

In this paper, we report the incorporation of PZT as the gate dielectric into ZnO NW FET. The schematic diagram of the device and a SEM image of a single ZnO NW FeFET are shown in Figure 1a,b, respectively. ZnO is a wide direct band gap (3.37 eV at room temperature) semiconductor with a large exciton binding energy (60 meV). ZnO NWs exhibit multifunctionality such as optoelectronics devices,[14] gas sensing,[15,16] and piezoelectricity.[17,18] Moreover, ZnO is a natural n-type semiconductor due to the presence of intrinsic donor-type defects such as oxygen vacancies and Zn interstitials.[19] Hence ZnO NWs can serve as the n-channel of a FET without intentional doping.[8,20]

Our NW FeFET device shows an evident $I_{ds}-V_g$ hysteresis with a current on/off ratio of $\sim 10^3$ and an endurance up to 10^3 cycles with little degradation. By comparing with conventional SiO_2 back-gate device, we attribute the memory effect to the reversible carrier concentration in the ZnO NWs modulated by remnant polarization switching of PZT. It is noted that similar memory effects have also been constructed using

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carbon nanotubes (CNTs) as the channel material, although the memory mechanism is under debate.[21−23]

Operation Mechanism of FeFET. The operation principle of the ZnO NW FeFET is proposed schematically in Figure 1c,d. First of all, unlike the conventional MOSFET that operates based on an inversion of the channel, our NW FET works in a depletion/accumulation mode. It is noted that among the large number of reported semiconducting NW FET devices, including NWs of Si, III−V, and metal oxides,[24−27] the NW channel is not inverted. Instead, the operating principle is accumulation/depletion of the NW as controlled by the gate potential. There have been only a few recent reports on inversion mode Si NW FET devices.[28−30] While it is expected that a wrap-gate NW FET should be more similar to conventional MOSFET,[31] the reported omega-shaped ZnO NW FET gates are still depletion mode ones.[26]

In the depletion mode, the gate electrostatic potential bends the channel's bands up or down, which brings the conduction band further away or closer to the Fermi level of the metal contacts. For a n-type NW such as ZnO, the energy bands are raised up when $V_g < 0$, causing a depletion of electrons in the NWs and thus decrease the conductivity. Conversely, $V_g > 0$ will lower the bands and enhance the conductivity.[8,27]

Coming to the NW FeFET, the operation mechanism is similar to conventional thin-film FET[11] except for a back-gate NW channel architecture. When a $-V_g$ pulse is applied between the NW channel and the Pt gate (*i.e.*, writing), the polarizations of the ferroelectric film will be aligned downward (Figure 1c). After the gate voltage pulse is removed, the remnant polarization of the ferroelectrics introduces an effective negative field effect, which induces an equal amount of positive space charges within the NW. This depletes the electrons in the channel (electron injection into the metal contacts), corresponding to an upward band bending at the NW/dielectric interface, and thus reduction of the conductance of the NW. This low conduction of the n-type ZnO NW FeFET represents a binary "0" state of the memory device. Reversely, when a $+V_g$ pulse is applied, a binary "1" state is obtained due to the enhanced conduction by electron accumulation. Thus a one-bit ferroelectric memory function is realized. A FeFET device allows nondestructive memory readout since the signal is read by detecting the conductance (or resistance) of the channel at zero gate voltage. The nonvolatile nature comes from the remnant polarization of the ferroelectric thin film, so that *reading* does not destroy the memory state.

Electric Transport Properties. The ferroelectric PZT film was characterized before device fabrication. The XRD pattern in Figure 2a was from the 200 nm thick film used in our study. A strong peak corresponding to PZT (111) can

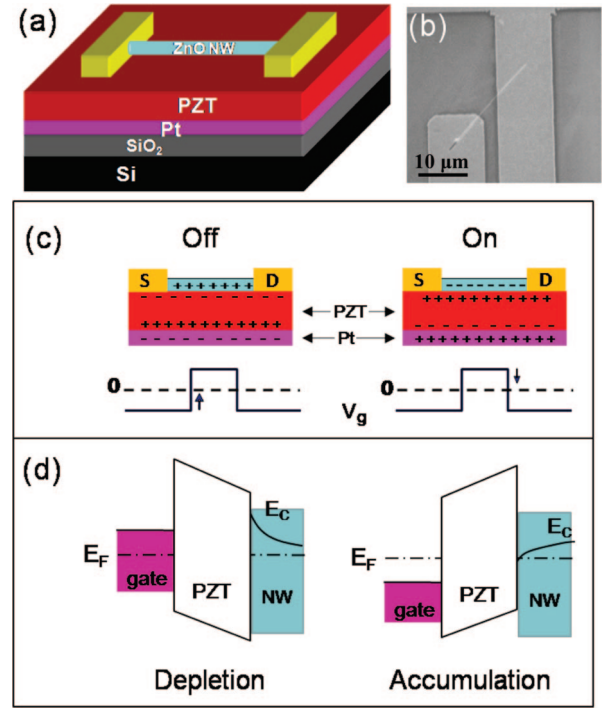

Figure 1. ZnO nanowire FeFET device. (a) Schematics of the device configuration. (b) SEM image of a single device. (c) Idealized field effect model of the ZnO nanowire FeFET device at "off" and "on" states, without considering surface and interface trap charges. (d) Corresponding band diagram showing the gate effect.

be identified together with two weaker peaks of (100) and (002). The full width at half-maximum of the PZT (111) rocking curve is as small as 4°. Hence it is indicated that the PZT film has a dominant orientation in <111>, which is a result of the well-known epitaxial growth of PZT on the (111)-oriented Pt layer. The film surface has

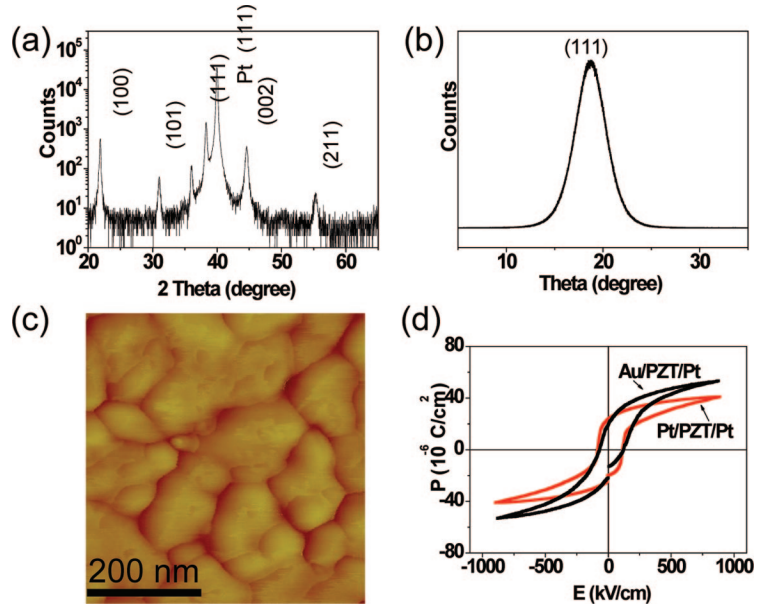

Figure 2. Evaluation of the PZT film. (a) XRD pattern of the film on the Pt/Ti/SiO_2/Si substrate. (b) X-ray rocking curve of the (111) plane. (c) AFM image of the film surface. (d) Typical *P*−*E* hysteresis loops of the capacitor structure based on Pt and Au top electrodes.

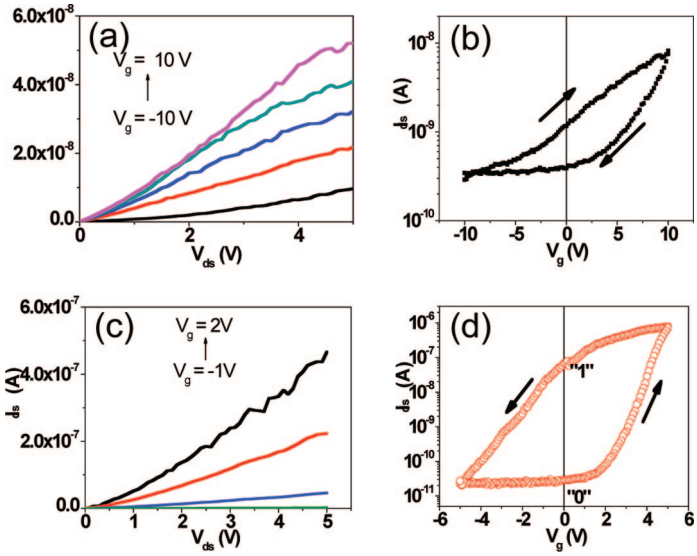

Figure 3. Electric transport properties of single ZnO nanowire FET devices at ambient condition. (a) $I_{ds}-V_{ds}$ output characteristics and (b) $I_{ds}-V_g$ transfer characteristics at V_{ds} = 2 V of a NW FET device on the SiO_2/Si substrate. (c) $I_{ds}-V_{ds}$ output characteristics and (d) $I_{ds}-V_g$ transfer characteristics at V_{ds} = 2 V of a FeFET device based on a ferroelectric PZT gate oxide.

a root-mean-square roughness of 10 nm, as revealed by the atomic force microscopic (AFM) image in Figure 2c. The polarization−electric field hysteresis loop of the PZT film is shown in Figure 2d, from which a remnant polarization (P_r) of 20 μC/cm^2 and a coercive field (E_c) of 100 kV/cm are determined. The PZT thin film exhibits a dielectric permittivity of 400, measured as a capacitor made by depositing the Pt top electrode on the PZT/Pt/Ti/SiO_2/Si substrate. Moreover, we also measured the polarization of the Au/PZT/Pt structrure, from which a remnant polarization (P_r) of 18 μC/cm^2 and a coercive field (E_c) of 80 kV/cm were determined.[32]

The overall device fabrication process involves (i) optimized growth of ZnO NWs and sol−gel deposition of PZT thin films, (ii) transfer of ZnO NWs directly from the growth substrate to the device substrate (PZT film or SiO_2/Si) *via* contact printing, and (iii) NW contacting using conventional sputtering, photolithography, and lift-off. Figure 1b gives a top view of a typical NW FeFET device.

For the electric properties, we start with a conventional NW FET on a 200 nm SiO_2/Si substrate as the back gate. Figure 3a shows the $I_{ds}-V_{ds}$ curves of a single NW FET. The conductance of the NW increases monotonically as the gate potential increases, demonstrating an n-channel ZnO NW FET. This is consistent with the natural n-type conductivity of ZnO due to the presence of intrinsic defects. Figure 3b plots the $I_{ds}-V_g$ curve of the same NW FET on a SiO_2 layer by sweeping the gate voltage continuously from −10 to 10 V at a rate of 0.2 V/s (the drain voltage is constant, V_{ds} = 2 V). A clockwise hysteresis loop is clearly observed, with a conductance change of about 3 times at zero V_g. The origin of such hysteresis is mainly due to the trap charges (see also below).[33]

Transport properties of ZnO NW FeFETs are shown in Figure 3c,d. On the basis of the $I_{ds}-V_{ds}$ output characteristics in Figure 3c, the conductance of the nanowire increased significantly as V_g varied from −1 to 2.0 V. Figure 3d shows the $I_{ds}-V_g$ transfer characteristic (scanning rate = 0.1 V/s, V_{ds} = 2 V). The threshold voltage varies from −5 to 2 V as the gate voltage sweeps upward and downward, respectively. The counterclockwise hysteresis loop is consistent with the expected memory effect of the ferroelectric film. A wide memory window of up to 7 V ensures its practical application potential.

Analogous to MOSFET, the transconductance (g_m) and the field effect electron mobility (μ) can be determined from the $I_{ds}-V_{ds}$ and $I_{ds}-V_g$ curves according to[34]

$$g_m = \frac{dI_{ds}}{dV_g}\Big|_{V_g=0} \quad (1)$$

$$\mu = g_m \frac{1}{C_{ox}} \frac{L^2}{V_{ds}} \quad (2)$$

which were first introduced to carbon nanotube (CNT) FET devices[34] and have also been commonly used for back-gated NW FETs.[24−27] C_{ox} is the gate oxide capacitance of a cylindrical wire on a planar substrate

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}[(r + t_{ox})/r]} \quad (3)$$

where ε_r is the relative dielectric constant (ε_r = 3.9 for SiO_2 and ∼400 for the PZT used here), t_{ox} is the thickness of gate oxide layer (200 nm), L is the channel length (3 μm), and r is the radius of the nanowire (50 nm). For NW FETs on the SiO_2/Si substrate, the threshold voltage V_{th} = 4 V and g_m = 1 nS can be extrapolated from the linear region of the $I_{ds}-V_g$ curve in Figure 4b. The mobility is $\mu_e \approx 20$ cm^2/V·s at V_g = 0 V. In case of the NW FeFET, similar calculation revealed that the differential conductance at V_{ds} = 2 V increased from 0.47 nS at V_g = −1 V to 100 nS at V_g = 2.0 V, and the mobility is about ∼72 cm^2/V·s at V_g = 0 V, with only a slight variation between different batches of the $I_{ds}-V_g$ loop measurements.

Furthermore, a significant difference of the subthreshold swing (S), defined as $S = \ln(10)[dV_g/d(\ln I)]$ between the ZnO NW FET and FeFET is noted. With 200 nm SiO_2 gate dielectric, the NW FET exhibits a swing of S = 5 V/dec. In contrast, with the 200 nm PZT dielectric, the NW FeFET shows S = 1 V/dec. As an important parameter of FET, subthreshold swing is desired to be small for low power operation. In this regard, the ZnO NW transistor with the PZT dielectric performs better than that with SiO_2.

The hysteresis in the $I-V_g$ curve allows us to define two states (denoted states "1" and "0") at V_g = 0 for the memory operation, as shown in Figure 3d. The remnant polarization difference is estimated to be ΔP = 36 μC/cm^2. The remnant polarization induces equal

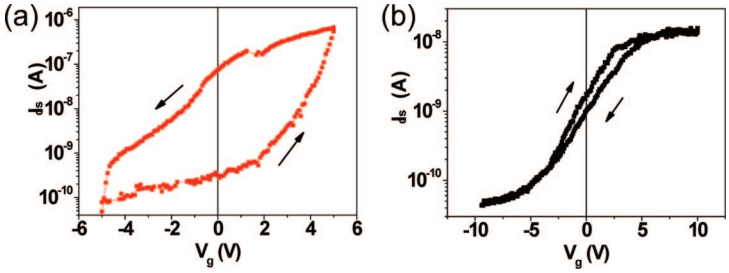

Figure 4. Transfer characteristics of the field effect devices measured at 150 °C (V_{ds} = 2 V). (a) Single ZnO nanowire FeFET. (b) Conventional FET on the SiO_2/Si substrate.

amounts of charges per unit area in the NW channel, and hence the difference in the charge density between state "1" and "0" is $\Delta Q_s = \Delta P = 36\ \mu C/cm^2$. Based on this, we can estimate the drain current in the low V_{ds} regime of output operation (neglecting the influence of interface states or contact resistance)[35]

$$I_{ds} = \mu \Delta Q V_{ds} W/L \quad (4)$$

where W is the effective channel width (78.5 nm).[5] The calculated I_{ds} at V_{ds} = 2 V is about 130 nA, larger than the experimental value of ~80 nA.

To exclude the possible effect by adsorption of a water liquid layer, we measured the $I-V_g$ curves at 150 °C (see Figure 4). By comparison to Figure 3, the hysteresis behavior of ZnO FeFET on the ferroelectric substrate shows little difference from that measured at room temperature, whereas the loop of FET on the SiO_2 substrate nearly vanishes.

The current rentention was also evaluated by monitoring the *off*- and *on*-state currents as a function of time after the gate programming. The drain currents were continuously monitored by measuring I_{ds} at a fixed V_{ds} = 2 V when the gate $V_g = \pm 5$ V was switched off (recall that the coercive voltage for the 200 nm PZT film is ±2 V). As shown in Figure 5a, for a device on the PZT film, the *on*-state current can stay at ~100 nA for about 200 s, and the persistence of the *off* state was about 120 s for PZT film. In contrast, both the *on* and *off* currents for the FET on the SiO_2 substrate start to relax after 5 s (Figure 5b). Although the retention time of our NW FeFET is still much shorter than the thin-film FeFET and other CNT-based FET memory devices (which are in the order of weeks), this is a proof-of-principle demonstration of the nonvolatile memory functionality of the ZnO NW FeRAM.

The endurance of the device is carried out by testing the drain current stability as a function of cycles. Both the *off*- and *on*-state currents were measured at a fixed V_{ds} = 2 V in the pause between gate voltage steps (*i.e.*, after each 1 s writing pulse by $V_g = \pm 5$ V). Each cycle lasts for 20 s. From results shown in Figure 6a, the *on*-state drain current is initially about 100 nA and stabilizes at 80 nA after more than 100 pulse cycles. When the device was poled with a pulse of −5 V, the *off*-state drain current was measured at an initial value of about 0.01 nA. It gradually reaches 0.5 nA after 200 cycles, partly due to the well-known fatigue problem of PZT. Based on Figure 6, the current on/off ratio remains ~200 after 300 readings.

For comparison, the memory endurance of the ZnO NW FET on SiO_2/Si is shown in Figure 6b. The pulsed measurement was conducted at V_{ds} = 5 V between the gate voltage pauses (the NW FET is "switched" by a gate voltage $V_g = \pm 10$ V). In contrast to the NW FeFET, the decrease in the *on* current and increase in the *off* current are more significant. The hysteresis degrades and completely disappears after 200 cycles. This indicates that the charge traps at the NW/SiO_2 interface are unstable during the cycling test. Among other reasons, water-related charge traps such as water molecules might be removed by thermal effect introduced by cycling $I-V$ measurement in a dry atmosphere.[36]

Discussion on Memory Effect. Depending on the material selection and interface quality, trap charges can be the main factor in the conductance hysteresis which has been observed in CNT FET[37−39] and Si NW FET[29] with SiO_2/Si back gates. The common types of charge traps include (1) SiO_2/Si interface trapped charges due to immobile oxide charges; (2) mobile ionic charge due to alkaline ion (*e.g.*, Na^+) contaminants that can be manipulated by bias-temperature aging; and (3) oxide-trapped space charge associated with defects in SiO_2. For example, Paruch *et al.* observed a pronounced hysteresis of CNT-based FeFET, which was attributed to charge injection into surface states of the ferroelectric $BaTiO_3$.[23] Similarly, in a recent article (published after the submission of the present paper) by Rinkio *et al.*,[39] surround-deposited HfO_2 was used as the gate dielectric of the CNT-based memory FETs, in which the stationary charge traps within HfO_2 dominate the hysteresis. In the thin-film FeFET based on a SnO_2 channel evaluated by Titkov *et al.*,[40] the density of trap charges is far higher than that of surface charge density in the channel, so

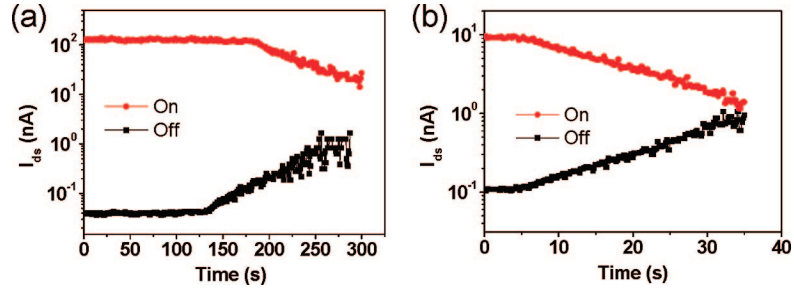

Figure 5. Time evolution of the drain currents of the ZnO nanowire-based FET devices. (a) FeFET. (b) Conventional FET on SiO_2/Si substrate; V_{ds} = 2 V. The gate pulse was ±5 V for (a) and ±10 V for (b).

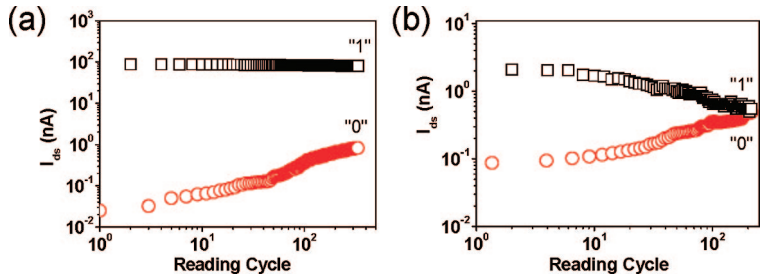

Figure 6. Endurance tests by measuring the *off*- and *on*-state drain current at a fixed V_{ds} = 2 V as a function of programming cycles of the ZnO nanowire-based FET devices. (a) FeFET. (b) Conventional FET on SiO_2/Si substrate. Circles and squares denote the current after the device is switched *on* and *off*, respectively.

that the former played the dominating role in the observed conduction hysteresis over the latter. Moreover, water charge traps have also been observed in MOS capacitances and tunnel diodes with hydrated SiO_2 gate insulators.[36,41,42]

We argue that the memory function of our NW FeFET originates mainly from the nature of the PZT ferroelectrics. First, the counterclockwise hysteresis for continuous V_g sweeps (Figure 3d) and the current levels by the pulsed measurement (*i.e.*, "on" current after positive V_g, whereas "off" current after negative V_g; see Figure 4a) are consistent with what would be expected for a ferroelectric field-effect modulation of an n-type channel. A hysteresis due to interface trap charges will be in the clockwise direction, as verified in this study (see Figure 3b). Second, *ex situ* deposition of NWs or CNTs on free surfaces of ferroelectrics (or other high-*k* oxides) and the measurements in ambient conditions are usually accompanied by non-negligible effects due to surface molecule adsorption (it has been shown that the adsorption can be ferroelectric polarization dependent[43]). The $I-V_g$ hysteresis behavior of our NW FeFET measured at 150 °C shows little difference, indicating the water liquid layer, if present, is not the main contribution. Finally, the increased conductance modulation compared to that of normal NW FETs with SiO_2/Si (see Figure 3) and the improved retention time (see Figure 5) also support that the ferroelectric field effect is the dominating source for the memory behavior.

In summary, ferroelectric FET devices using a semiconducting ZnO nanowire as the n-type channel have been fabricated and evaluated with a comparison to conventional SiO_2 back-gated NW FETs. The transistors exhibit enhanced electric transport properties compared to transistors using SiO_2 gate oxide, as a result of the high dielectric constant of the PZT thin film. In addition, a memory effect is demonstrated with a current on/off ratio at zero gate voltage up to 10^3 and a memory window of ~7 V. We argue that the memory property is associated with the bistable permanent polarization of the ferroelectric PZT, which modulates the carrier concentration, and hence the conductance, of the ZnO nanowires reversibly.

While our result implies that such a NW channel FeFET device is promising for RAM applications, it still has large room for improvement. Prospectively, if the sol−gel polycrystalline PZT is replaced by the higher-quality epitaxial single-crystalline PZT films,[44] it is expected that the performance would be further enhanced in terms of retention and fatigue. Further, a lateral homogeneous modulation is possible if the ferroelectric dielectric layer can be deposited around the nanowires in core/shell geometry, together with a wrap-around gate.[45]

METHODS

The $Pb(Zr_{0.3}Ti_{0.7})O_3$ thin films were deposited *via* a sol−gel route,[46] assisted by spin coating. The precursor was prepared from $Pb(CH_3COO)_23H_2O$, $Zr[OCH(CH_3)_2]_4$, and $Ti[OCH(CH_3)_2]_4$. The starting materials were dissolved in a solvent mixture consisting of ethylene glycol monomethyl ether ($C_3H_8O_2$) and acetic acid (solvent volume ratio = 5/1.3). The concentration of the sol solution was controlled at 0.4 M. The $PZ_{30}T_{70}$ precursor solution was first spin-coated on the Pt/Ti/SiO_2/Si substrate at 3000 rpm for 30 s to form the first layer, followed by drying at 300 °C for 5 min on a hot plate, and baking at 500 °C for 5 min. The PZT films were annealed at a temperature in the range of 600−700 °C for 1 h in a quartz furnace to realize the wanted perovskite structure.

The ZnO nanowires were grown by a catalyst-assisted vapor transport method.[47] ZnO (99.99%, Alfa Aesar) and graphite (99.99%, Aldrich) powders (1:1 wt % ratio) were mixed and used as source. Si (111) substrates were precoated with a 2 nm Au films as catalyst. The source was placed in the center of a horizontal tube furnace maintained at 950 °C, and the substrate was placed at a temperature zone of 550 °C for collecting ZnO NWs. The microstructures and morphologies of ZnO NWs were characterized by X-ray diffraction (XRD, D8 Advanced), scanning electron microscopy (SEM, JEOL JSM-6700F), and transmission electron microscopy (TEM, 200kV JEOL 2010F).

The as-grown ZnO NWs were removed by sonication from the substrates and dispersed in ethanol. The solution was dripped on SiO_2/Si (*i.e.*, 200 nm insulated SiO_2 film over Si substrate) and PZT/Pt/Ti/SiO_2/Si substrates, and then Au contact pads of 100 nm thick were fabricated by photolithography and rf-sputtering. Finally, the devices were annealed at 350 °C in vacuum for producing good contacts. The surface morphology of the PZT film was characterized by atomic force microscopy (AFM, Veeco, Nanoscope V). The electrical transport properties were measured by Suss probe station with Keithley 4200 SCS. Their ferroelectric and dielectric properties were characterized using a ferroelectric analyzer (Radiant Technologies) and impedance analyzer (Solartron SI 1260, UK).

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